a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

73. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said interconnection and being connected with one of said source region and said drain region, said layer comprising metal being connected with said interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

74. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

75. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

76. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to ~~said channe~~l region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising metal provided on said insulating surface and being in direct contact with said interconnection and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising metal;

a contact hole provided over said layer comprising metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said contact hole.

81. (Amended) The device of claim 74 wherein said layer comprising metal is connected with said interconnection through no contact hole.

83. (Amended) The device of claim 75 wherein said layer comprising metal is connected with said interconnection through no contact hole.

85. (Amended) The device of claim 76 wherein said layer comprising metal is connected with said interconnection through no contact hole.

86. (Amended) A display device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising said metal provided on said insulating surface and being in direct contact with said interconnection

and being connected with one of said source region and said drain region;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.

87. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

an interconnection formed on said insulating surface;

a layer comprising said metal provided on said insulating surface and being in direct contact with said interconnection

and being connected with one of said source region and said drain region, said layer comprising said metal being connected with said interconnection through no contact hole;

an interlayer dielectric provided over said gate electrode and said layer comprising said metal;

a contact hole provided over said layer comprising said metal in said interlayer dielectric; and

a top layer interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising said metal through said contact hole.

Please add claims 88-101.

-- 88. (New) A display device according to claim 61, wherein a glass substrate has said insulating surface.

89. (New) A semiconductor device according to claim 73, wherein a glass substrate has said insulating surface.

90. (New) A semiconductor device according to claim 74, wherein a glass substrate has said insulating surface.

91. (New) A semiconductor device according to claim 75, wherein said substrate is a glass substrate.

92. (New) A semiconductor device according to claim 76, wherein said substrate is a glass substrate.

93. (New) A display device according to claim 86, wherein said substrate is a glass substrate.

94. (New) A semiconductor device according to claim 87, wherein a glass substrate has said insulating surface.

95. (New) A display device according to claim 61, wherein said interconnection is provided in a same layer as said gate electrode.

96. (New) A semiconductor device according to claim 73, wherein said interconnection is provided in a same layer as said gate electrode.

97. (New) A semiconductor device according to claim 74, wherein said interconnection is provided in a same layer as said gate electrode.

98. (New) A semiconductor device according to claim 75, wherein said interconnection is provided in a same layer as said gate electrode.

99. (New) A semiconductor device according to claim 76, wherein said interconnection is provided in a same layer as said gate electrode.

100. (New) A display device according to claim 86, wherein said interconnection is provided in a same layer as said gate electrode.

101. (New) A semiconductor device according to claim 87, wherein said interconnection is provided in a same layer as said gate electrode. --